Engine module

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Abbreviations

Abbr.	Description
ACI	Accessory Control Interface
ADC	Analog Digital Connector
ARM	Advanced RISC Machines
ASIC	Application Specific Integrated Circuit
ATR	Answer To Reset
BB	Baseband
BL-5C	Battery type.
BSI	Battery Size Indicator
Cbus	Control bus (internal phone interface between UPP-UEM)
CCS	Customer Care Service
CTI	Cover Type Indicator
CTSI	Clock Timing Sleep and Interrupt
Dbus	DSP controlled bus (Internal phone interface between UPP-UEM)
DC	Direct Current
DCT4.0	Digital Core Technology, generation 4.0
DSP	Digital Signal Processor
DUT	Device under test
EAD	External Accessory Detection
EMC	Electro Magnetic Compatibility
ESD	Electro Static Discharge
Fbus	Fast Bus, asynchronous message bus connected to DSP (communications bus)
FCI	Functional cover interface
FPC	Flexible printed circuit
FR	Full Rate
GENIO	General Purpose Input/Output
GSM	Global System Mobile

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HW	Hardware
IF	Interface
IHF	Integrated Hands Free
IMEI	International Mobile Equipment Identity
LCD	Liquid Crystal Display
LDO	Low Drop Out
LED	Light Emitting Diode
Li-Ion	Lithium Ion battery
LPRF	Low Power Radio Frequency
Lynx	Battery type
MALT	Medium And Loud Transducer
Mbus	Asynchronous message bus connected to MCU (phone control interface). Slow message bus for control data.
MCU	Micro Controller Unit
NO_SUPPLY	UEM state where UEM has no supply what so ever
NRT	Nokia Ringing Tones
NTC	Negative temperature Coefficient, temperature sensitive resistor used as a temperature sensor.
PA	Power Amplifier (RF)
PDM	Pulse Density Modulation
PDRAM	Program/Data RAM
Phoenix	SW tool of DCT4.x
PLL	Phase locked loop
PnPHF	Plug and Play Handsfree
PUP	General Purpose IO (**P**IO), **U**SARTS and **P**ulse Width Modulators
PWB	Printed Wired Board
PWR_OFF	UEM state where phone is off
PWRONX	Signal from power on key.
R&D	Research and development
RESET	UEM state where regulators are enabled
RTC	UEM internal Real Time Clock

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SARAM	Single Access RAM
SIM	Subscriber Identification Module
SLEEP	UEM power saving state controlled by UPP
SPR	Standard Product Requirements
SRAM	Static RAM
STI	Serial Trace Interface
SW	Software
TBSF	Through the Board Side Firing
TI	Texas Instruments, American company
UEM	Universal Energy Management
UI	User Interface
UPP	Universal Phone Processor
VBAT	Main battery voltage
VCHAR	Charger input voltage
VCHARDET	Charger detection threshold level
VMSTR+, VMSTR	Master Reset threshold level

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Baseband HW Introduction

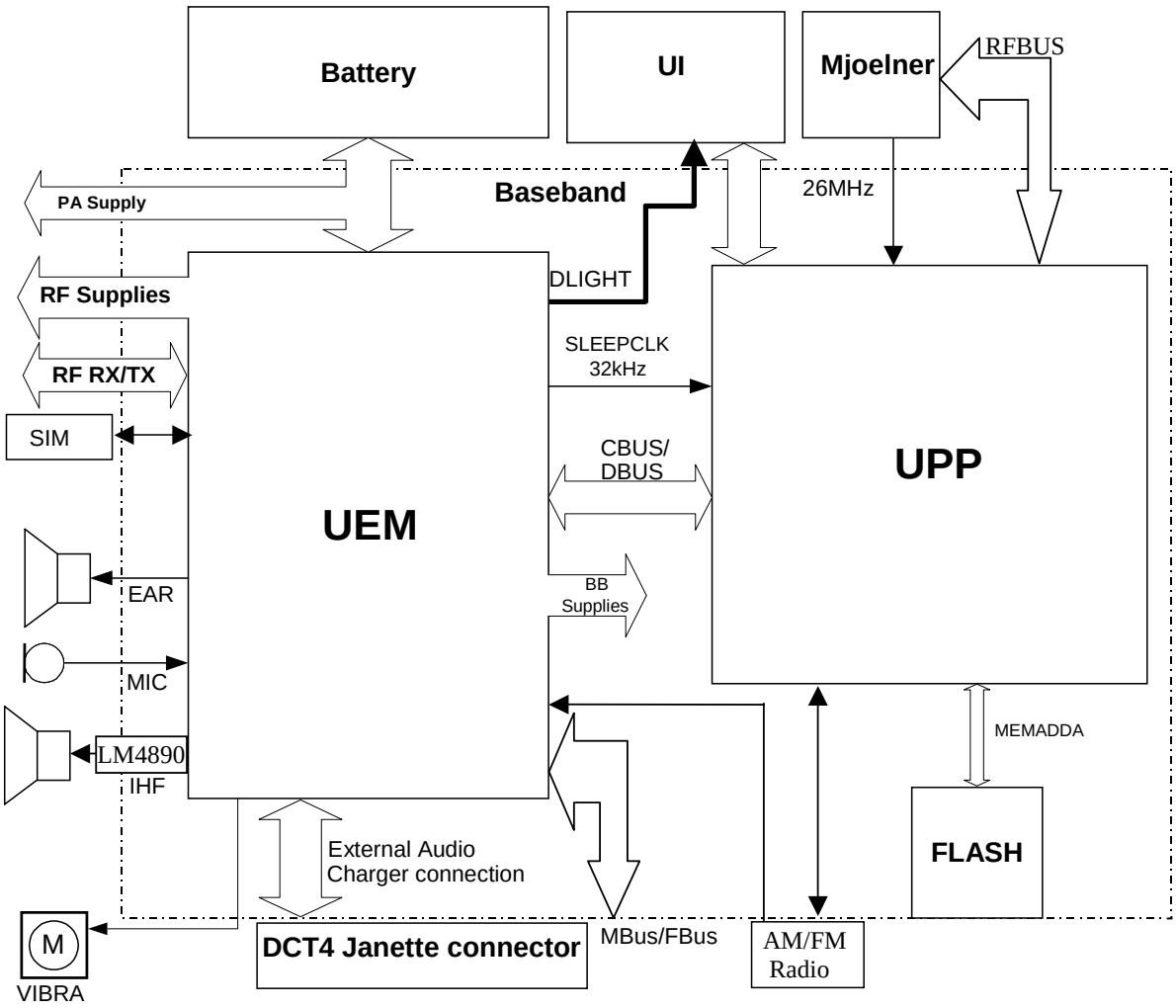
This document specifies the baseband module for the Nokia 2300 phone. The baseband module includes the baseband engine chipset, the UI components and the acoustical parts for the transceiver.

Nokia 2300 is a hand-portable dual band 900/1800MHz phone, featuring DCT4 generation baseband (UEM/UPP) and RF (MJOELNER) circuitry. Nokia 2300 is closely related to Nokia 3510 and 3510i

Technical Summary

The baseband module contains 2 main ASICs named UEM and UPP. The baseband module furthermore contains a Flash IC of 16Mbit. The baseband is based on the DCT4 engine program.

Figure 1: Nokia 2300 baseband block diagram



The UEM supplies both the baseband module as well as the RF module with a series of voltage regulators. Both, the RF and baseband modules are supplied with regulated voltages of 2.78V and 1.8V. The UEM includes 6 linear LDO (low drop-out) regulators for baseband and 7 regulators for RF. The UEM is furthermore supplying the baseband SIM interface with a program-

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mable voltage of either 1.8 V or 3.0 V. The core of the UPP is supplied with a programmable voltage of 1.0 V, 1.3 V, 1.5 V or 1.8 V.

The UPP operates from a 26MHz clock, coming from the RF ASIC MJOELNER, the 26 MHz clock is internally divided by two, to the nominal system clock of 13MHz. The DSP and MCU contain phase locked loop (PLL) clock multipliers, which can multiply the system frequency.

The UEM contains a real-time clock, sliced down from the 32768 Hz crystal oscillator. The 32768 Hz clock is fed to the UPP as a sleep clock.

Communication between the UEM and the UPP is carried out via the bi-directional serial buses CBUS and DBUS. The CBUS is controlled by the MCU and it operates at a speed of 1 MHz set by SW. The DBUS is controlled by the DSP and it operates at a speed of 13 MHz. Both processors are located in the UPP.

The UEM ASIC mainly handles the interface between the baseband and the RF section**.** The UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The UEM supplies the analog signals to RF section according to the UPP DSP digital control.

The RF ASIC MJOELNER is controlled through the UPP RFBUS serial interface. There are also separate signals for PDM coded audio. Digital speech processing is handled by the DSP inside the UPP ASIC. The UEM is a dual voltage circuit, the digital parts are running from the baseband supply 1.8V and the analog parts are running from the analog supply 2.78V, VBAT is directly used by some blocks also.

The baseband supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is carried out by the UEM according to control messages from the UPP.

Nokia 2300 has two external serial control interfaces: FBUS and MBUS. These buses can be accessed only through the production test pattern as described in section 4.

The transceiver module is implemented on 6 layer selective OSP/Gold coated PWB.

Modes of Operation

Nokia 2300 baseband engine has six different operating modes (in normal mode):

- No_Supply
- Power_off
- Acting_Dead
- Active
- Sleep
- Charging

Additionally, two modes exist for product verification: 'test mode' and 'local mode'.

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No supply

In No_Supply mode, the phone has no supply voltage. This mode is due to disconnection of the main battery or low battery voltage level.

The phone is exiting from No_Supply mode when sufficient battery voltage level is detected. Battery voltage can rise either by connecting a new battery with VBAT > V_{mstr+} or by connecting charger and charging the battery above V_{mstr+}.

Power_off

In this state the phone is powered off, but supplied. The VRTC regulator is active (enabled) having supply voltage from the main battery. Note that the RTC status in the PWR_OFF mode depends on whether RTC was enabled or not when entering PWR_OFF. From the Power_off mode the UEM enters the RESET mode (after 20ms delay), if any of the following statements is true (logical OR –function):

- Power_on button detected (PWROFFX)
- charger connection detected (VCHARDET)
- RTC_ALARM detected

The phone enters the POWER_OFF mode from all the other modes except NO_SUPPLY if the internal watchdog elapses.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called ”Acting Dead”. In this mode no RF parts are powered. To the user, the phone acts as if it was switched off. A battery-charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

In active mode SW controls the RF regulators.

Table 1: Regulator controls

Regulator	NOTE
VFLASH1	Enabled; Low Iq mode during sleep
VFLASH2	Enabled; Disabled in sleep mode; Used for FM radio
VANA	Enabled; Disabled in sleep mode
VIO	Enabled; Low Iq mode during sleep
VCORE	Enabled; Low Iq mode during sleep
VSIM	Controlled by register writing.

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Table 1: Regulator controls

VR1A	Enabled; Disabled in sleep mode
VR1B	Not used in Nokia 2300, disabled
VR2	Controlled by register writing; Enabled in sleep mode
VR3	Enabled; Disabled in sleep mode
VR4	Not used in Nokia 2300, disabled
VR5	Enabled; Disabled in sleep mode
VR6	Enabled; Disabled in sleep mode
VR7	Enabled; Disabled in sleep mode
IPA1-2	Not used in Nokia 2300, disabled

Sleep mode

The sleep mode is entered when both MCU and DSP are in stand-by mode. Sleep is controlled by both processors. When SLEEPX low signal is detected, the UEM enters SLEEP mode. VCORE, VIO and VFLASH1 regulators are put into low quiescent current mode. All RF regulators, except VR2, are disabled in SLEEP. When SLEEPX=1 is detected UEM enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection etc.

In the sleep mode, the main oscillator (26MHz) is shut down and the 32kHz sleep clock oscillator is used as a reference clock for the baseband.

Charging

Charging can be performed in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity and technology.

The battery voltage, temperature, size and current are measured by the UEM controlled by the charging software running in the UPP.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

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DC Characteristics

Supply Voltage Ranges

Table 2: Absolute Maximum Ratings

Signal	Rating
Battery Voltage	0 ... 4.39V (VBAT)
Charger Input Voltage	-0.3 ... 9.2VRMS (16,9 Vpeak)

Following voltages are assumed as normal and extreme voltages for used battery:

Table 3: Battery voltage range

Signal	Min	Nom	Max	Note
VBAT	3.21V	3.80V	4.39V	[1]
Vcoff+	3.0V	3.1	3.2	HW off to on
Vcoff-	2.7V	2.8V	2.9V	HW on to off
Vmstr+	2.0V	2.1V	2.2V	UEM off to on
Vmstr-	1.8V	1.9V	2.0V	UEM on to off
Sw shutdown	-	3.1V	-	In Call
Sw shutdown	-	3.2V	-	In Idle

[1] According to the GSM specifications, a GSM device with a Li-ion battery should work correctly if it is powered by its nominal voltage +/-15%. The UEM hardware shutdown is from 3.10V and below. The Energy Management of this phone shuts the phone down at 3.20V in order to perform a correct shutdown of the phone. Above 3.20V + tolerances, at 3.21V, the phone is still fullfilling all the GSM requirements. The nominal voltage is therefore set at 3.80V. This is higher than the normal battery voltage and is only set so that the phone is fullfilling Type Approval. Some of BB testing might be done on battery level.
During fast charging of an empty battery voltages between 4.20 and 4.60 might appear for a short while.

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Regulator Voltage Ranges

Table 4: BB regulators

Signal	Min	Nom	Max
VANA	2.70V	2.78V	2.86V
VFLASH1	2.70V	2.78V	2.86V
VFLASH2	2.70V	2.78V	2.86V
VSIM	1.745V 2.91V	1.8V 3.0V	1.855V 3.09V
VIO	1.72V	1.8V	1.88V
VCORE	1.000V 1.140V 1.235V 1.425V 1.710V	1.053V 1.2V 1.3V 1.5V 1.8V	1.106V 1.260V 1.365V 1.575V 1.890V

Table 5: RF regulators

Signal	Min	Nom	Max
VR1A	4.6V	4.75V	4.9V
VR1B	4.6V	4.75V	4.9V
VR2 V_{out_on} V_{out_sleep}	2.70V 2.61V	2.78V	2.86V 2.95V
VR3	2.70V	2.78V	2.86V
VR4	2.70V	2.78V	2.86V
VR5	2.70V	2.78V	2.86V
VR6	2.70V	2.78V	2.86V
VR7	2.70V	2.78V	2.86V

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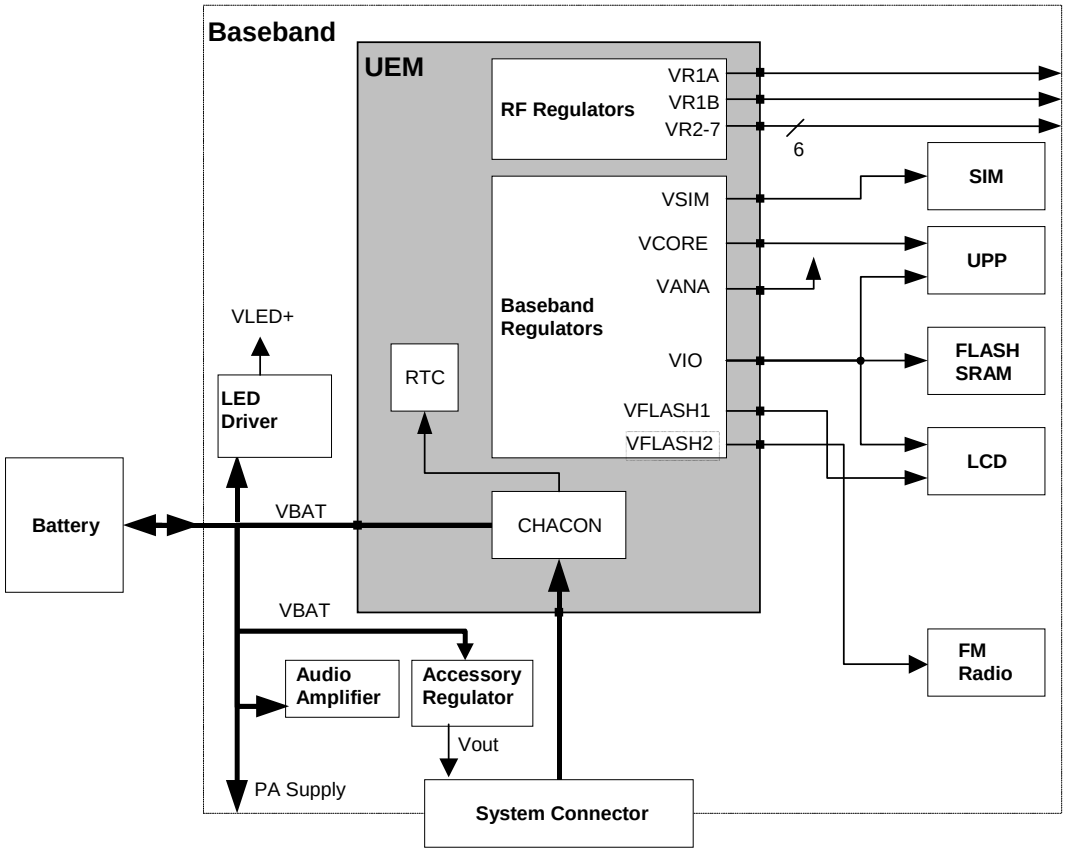
Interconnection Diagram

Figure 2: Power distribution diagram



External Signals and Connections

System connector (X102)

Table 6: DC connector

Pin	Signal	Min	Nom	Max	Condition	Note
2	VCHAR	-	11.1V_{peak}	16.9 V_{peak} 7.9 V_{RMS} 1.0 A_{peak}	Standard charger (ACP-7)	Charger positive input
		7.0 V_{RMS}	8.4 V_{RMS}	9.2 V_{RMS} 850 mA	Fast charger	
1	CHGND	-	0	-		Charger ground

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Table 7: External microphone

Signal	Min	Nom	Max	Condition	Note
MIC2P (Differential input P)	-	-	100mV$_{pp}$	G=20dB	1,22kΩ to MIC1B (AC condition)
MIC2N (Differential input N)	-	-	100mV$_{pp}$	G=20dB	1kΩ to GND
MICB2 (Microphone Bias)	2.0 V	2.1 V	2.25 V	DC	Unloaded
External loading of MICB2	-	-	600uA	DC	

Table 8: External speaker, differential output XEARP (HF) & XEARN (HFCM)

Signal	Min	Nom	Max	Units	Note
Output voltage swing* * seen from transducer side	2.0	-	-	Vpp	Differential output, with 60 dB signal to total distortion ratio
Common voltage level for HF output (HF & HFCM) VCMHF	0.75	0.8	0.85	V	
Load Resistance (HF to HFCM)	154	194	234	W	2×22Ω (±5%) + 150Ω (±25%)
Load Capacitance (HF to HFCM)	-	-	10	NF	Load to GND

Table 9: Headset detection

Signal	Min	Nom	Max	Condition	Note
HookInt	0V	-	2.86V (Vflash1)		Headset button call control, connected to UEM AD-converter
HeadInt	0V	-	2.86V (V flash1)		Accessory detection, connected to UEM AD-converter

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Battery connector

Name	Description	Test usage
VBAT	Battery voltage terminal.	Battery calibration.
GND	Battery ground terminal.	
BSI	Battery size identification.	Flash and local mode forcing.

Battery temperature is estimated by measurement in transceiver PWB with a separate NTC resistor.

Baseband – RF interface

The interface between the baseband and the RF can be divided into three categories:

- The digital interface from the UPP to the RF ASIC (Mjoelner). The serial digital interface is used to control the operation of the different blocks in the RF ASICs.
- The analogue interface between the UEM and RF. The analogue interface consists of RX and TX converter signals. The power amplifier control signal TXC and the AFC signal come from the UEM as well.
- Reference clock interface between Mjoelner and UPP which supplies the 26Mhz system clock for the UPP.

Internal Signals and Connections

The tables below describe internal signals. The signal names can be found on the schematic for the PWB.

Audio

Table 10: Internal microphone

Signal	Min	Nom	Max	Condition	Note
MIC1P (Differential input P)	-	5mV	-	G=0dB	1kΩ to MIC1B (RC filtered by 220R/ 4.7uF)
MIC1N (Differential input N)	-	5mV	-	G=0dB	1kΩ to GND
MICB1 (Microphone Bias)	2.0 V	2.1 V	2.25 V	DC	
External loading of MICB1	-	-	600uA	DC	

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Table 11: Internal speaker (Differential output EARP & EARN)

Signal	Min	Nom	Max	Units	Note
Output voltage swing	4.0	-	-	Vpp	Differential output
Load Resistance (EARP to EARN)	26	32	-	W	
Load Capacitance (EARP to EARN)	-	-	50	NF	

Speaker (IHF & ringer)

Table 12: Connections between UPP and Boomer

Signal	From	To	Parameter	Min.	Max.	Unit	Notes
Shutdown	GENIO[14]	Shutdown (p. 5)	Vih Vil	1.2 -	- 0.4	V V	Boomer Shut-down thresh-old levels

Table 13: Connections between UEM/Battery and LM4890

Signal name	From	To	Parameter	Min.	Max.	Unit	Notes
XAUDIO[1] Filtered sig-nal	Differential between HF and HFCM. No direct connection between UEM and LM4890	LM4890	Output Swing	-	80mV	Vpp	Long-term consumption
VBAT	Battery	LM4890 (p. 6)	Supply	3.1	4.39	V	Lower limit is SW cut-off

Baseband board clocks

Table 14: Board Clocks

Signal name	From	To	Min.	Typ.	Max.	Unit	Notes
RFCLK	MJOELNER	UPP	-	26	-	MHz	Active when SLEEPX is high
SLEEPCLK	UEM	UPP	-	32.768	-	KHz	Active when VBAT is supplied
RFCONVCLK	UPP	UEM		13	-	MHz	Active when RF converters are active

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Table 14: Board Clocks

RFBUSCLK	UPP	MJOELNER	-	13	13	MHz	Only active when bus-enable is active
DBUSCLK	UPP (DSP)	UEM	-	13	13	MHz	Only active when bus-enable is active
CBUSCLK	UPP (MCU)	UEM	-	1	1.2	MHz	Only active when bus-enable is active
LCDCAMCLK	UPP (Write) (Read)	LCD	0.3	 3.25 0.650	4	MHz	Only active when bus-enable is active

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Environmental Specifications

Operating conditions

Temperature Conditions

Table 15: Temperature conditions for Nokia 2300

Environmental condition	Ambient temperature	Remarks
Normal operation	-25 ° C … +55 °C	Specifications fulfilled
Reduced performance	-40 °C ..-25 °C and +55 °C … +85 °C	
No operation and/or storage	< -40 °C or > +85 °C	No storage or operation. An attempt to operate may damage the phone permanently

Humidity

The Nokia 2300 BB module is not protected against water. Condensed or splashed water might cause malfunction. Any submerge of the phone will cause permanent damage. Long-term high humidity, with condensation, will cause permanent damage because of corrosion.

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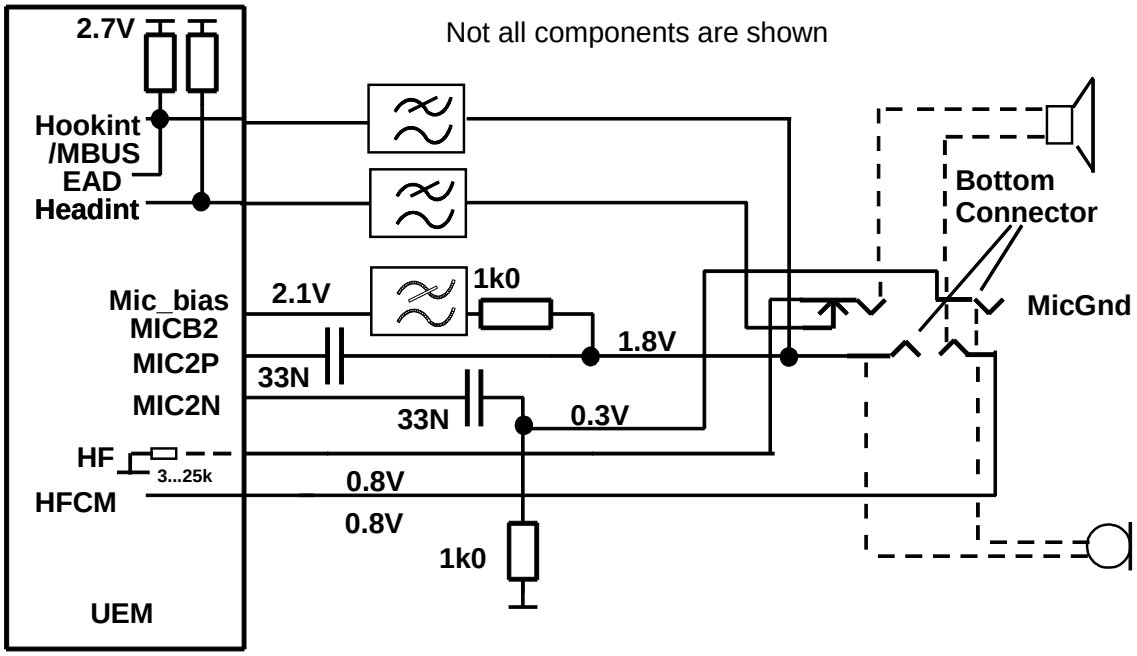
Functional Description

Audio External

Nokia 2300 is designed to support a fully differential external audio accessory connection. A headset and PnPHF can be directly connected to the system connector. Detection of the different accessories is made in an analogue way by reading the DC voltage value of EAD converter.

Figure 3: Headset interface



Audio Internal

Earpiece

The earpiece selected is a 13 mm dynamic earpiece with a nominal impedance of 32 Ω (previously used for 3210, 3310, 6210, among others).

The earpiece is placed within the mechanical parts, e.g. C-cover and Light guide. The holes of the A-cover and the choice of dust shield are made in a way to have the best transmission of the sound, without having much impact on the sound waves and sound qualities.

The acoustic design involves a sandwich of five parts: Earmat, A-cover, C-cover, lightguide- and D-cover.

On top of the lightguide there will be a metal frame (C-cover) that will protect the earpiece. The C-cover will contain 5 acoustical holes and a double-sided gasket for sealing in the area over the earpiece.

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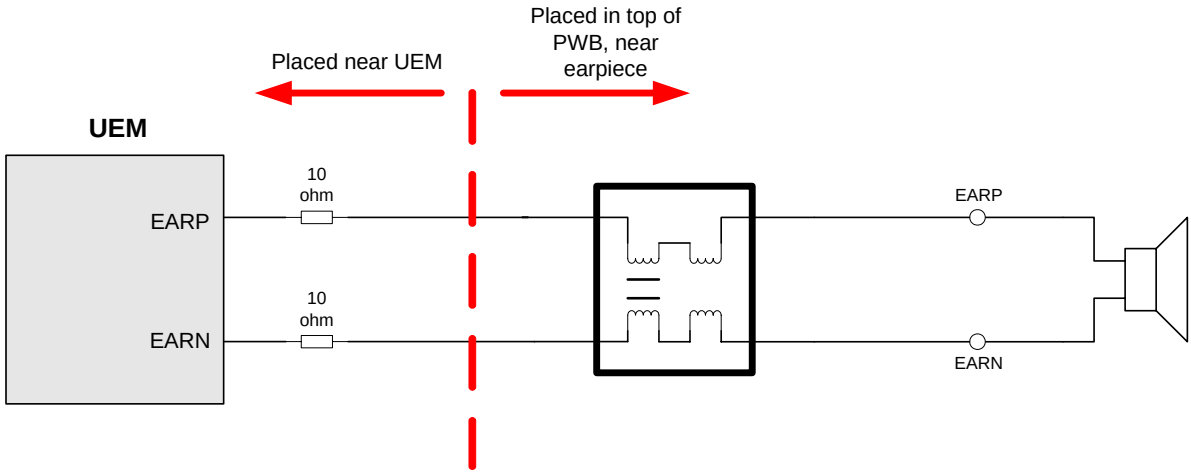
The front cover consists of two parts, an A-cover and an earmat.

The earpiece circuit includes only a few components:

- two 10 ohm in order to have a stable output
- an EMC filter

Figure 4: Earpiece interface

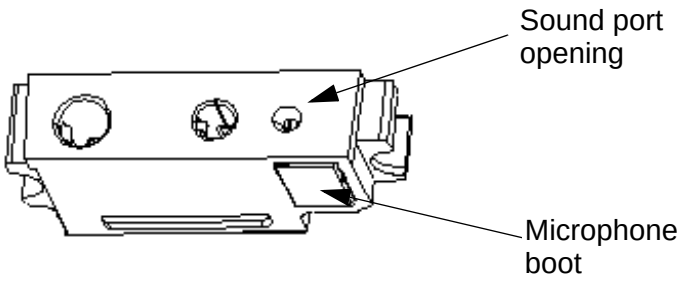


Microphone

Acoustical design

An omni directional microphone is used. The microphone is placed in the system connector sealed in its rubber gasket. The sound port is provided in the system connector. This design is well known from Nokia 3310. The only change done to the bottom connector is that the external charger pads were removed.

Figure 5: Bottom connector



Electrical interface

Nokia 2300 uses a differential bias circuit, driven directly from the MICB1 bias output with external RC filters.

The RC filter (220 Ω, 4.7µF) is scaled to provide damping at 217 Hz. 217 Hz audible noise (TDMA).

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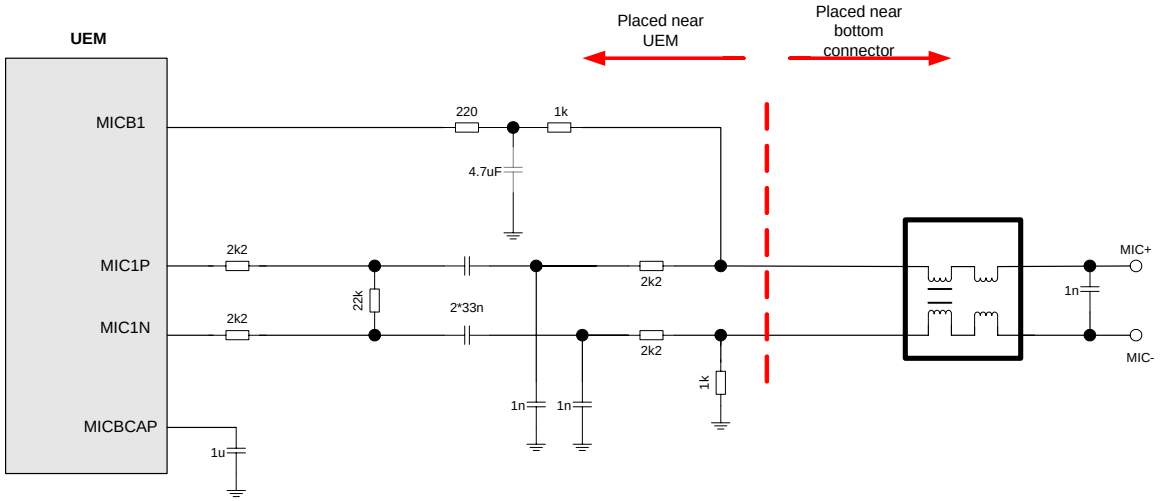
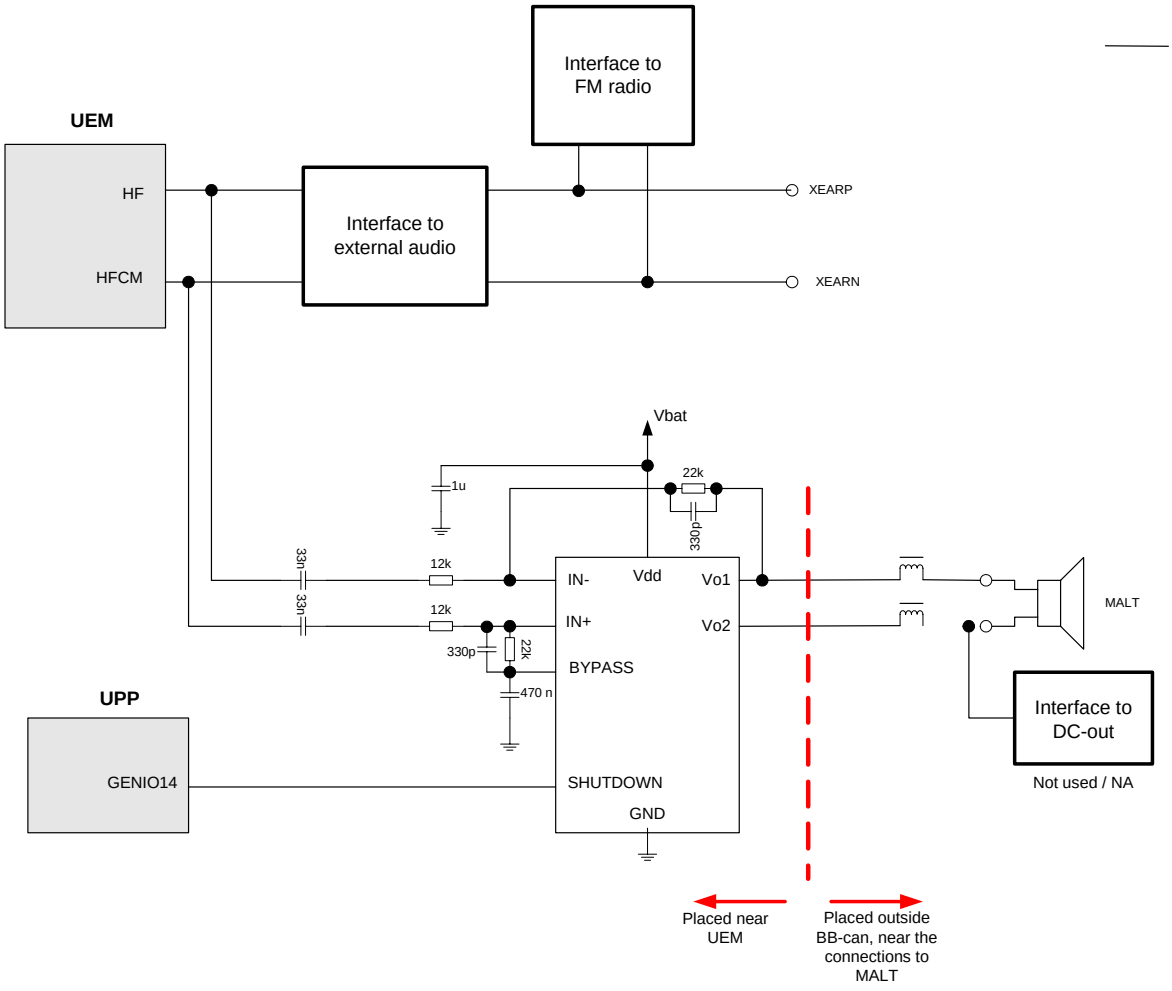
The RC filter 2.2 kΩ and 1nF are EMC component, while the remaining 10 nF and 1 nF capacitors near the bottom connector are for ESD.

Figure 6: Internal electrical microphone interface



Power amplifier (boomer)

Figure 7: Interface between the MIDI circuit and UEM



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The speaker has an external amplifier connected (a so-called boomer) to provide sufficient power for an 8 Ω load. The boomer is implemented with a differential configuration on the input. The inputs are wired to the headset connections HF and HFCM from UEM. These two outputs can each deliver an output swing up to 1.6 Vpp before clipping occurs. HF and HFCM are 180 × out of phase.

Under normal conditions HF and HFCM will be used for downlink audio to the headset/car kit. During headset/car kit usage, where the MIDI speaker is supposed not to be active, the MIDI amplifier can be disabled by means of the shutdown pin, which is controlled by changing the logic level on SHUTDOWN (managed by UPP). During sleep, keeping the shutdown pin "low" also secures a minimum amount of stand-by current to be consumed.

The SHUTDOWN pin shall be timed so that GENIO14 isn't enabled until the DC level shift on HF and HFCM have reached their permanent level (0.8 V_{DC}). This in order to remove click sounds in the MALT speaker. Furthermore, when a ringing tone is ending, SHUTDOWN shall be disabled before the DC level on HF and HFCM changes again.

Table 16: Control of SHUTDOWN.

	Accessory mode	HF-output of UEM	SHUTDOWN
In-coming call	No accessories connected	MIDI-tone routed to HF and HFCM	Logic "High"
	Accessories connected	MIDI-tone routed to HF and HFCM	Logic "High"
Conversation (non IHF)	No accessories connected	No audio routed to HF and HFCM	Logic "Low"
	Accessories connected	Downlink routed to HF and HFCM	Logic "Low"
Conversation (IHF)	No accessories used, or headset connected	Downlink routed to HF and HFCM	Logic "High"
	Car kit connected	No audio routed to HF and HFCM	Logic "Low"
Sleep	-	-	Logic "Low"

SHUTDOWN is an active high input.

The amplification for the given boomer configuration will be equal to 18.5 dB.

Batteries

Type: BL-5C

Technology: Li-Ion. 4.23V charging.

Capacity: 850 mA/h

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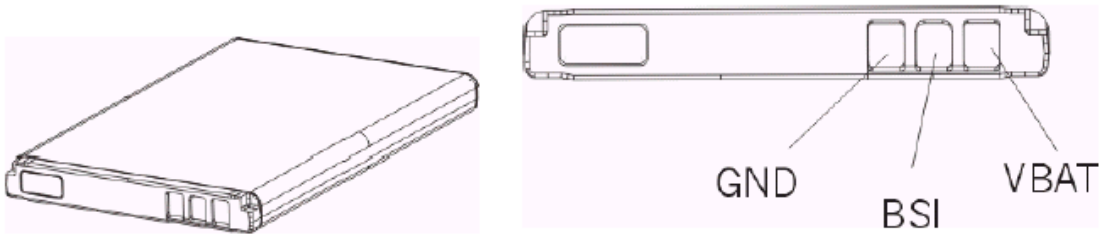
Figure 8: BL-5C battery



The BSI values for the BL-5C batteries:

Table 17: BSI levels BL-5C Battery

Mode	BSI (kOhm)			Description
	Min	Type	Max	
Normal		75		Used for calculating the Capacity (BL5-C = 850mA)
Service	3.2	3.3	3.4	Pull-down resistor in battery. Used for fast power-up in production (LOCAL mode), R/D purposes or in after sales, 1% tolerance resistors shall be used.
Test	6.7	6.8	6.9	Pull-down resistor in battery, used in production for testing purposes. 1% tolerance resistors shall be used.
Banned			<3.2	

Inside the battery, an over-temperature and an over-voltage protection circuit are present.

The BL-5C battery does not contain a temperature sensor. An external temperature sensor (NTC resistor) is placed on the PWB to measure the temperature.

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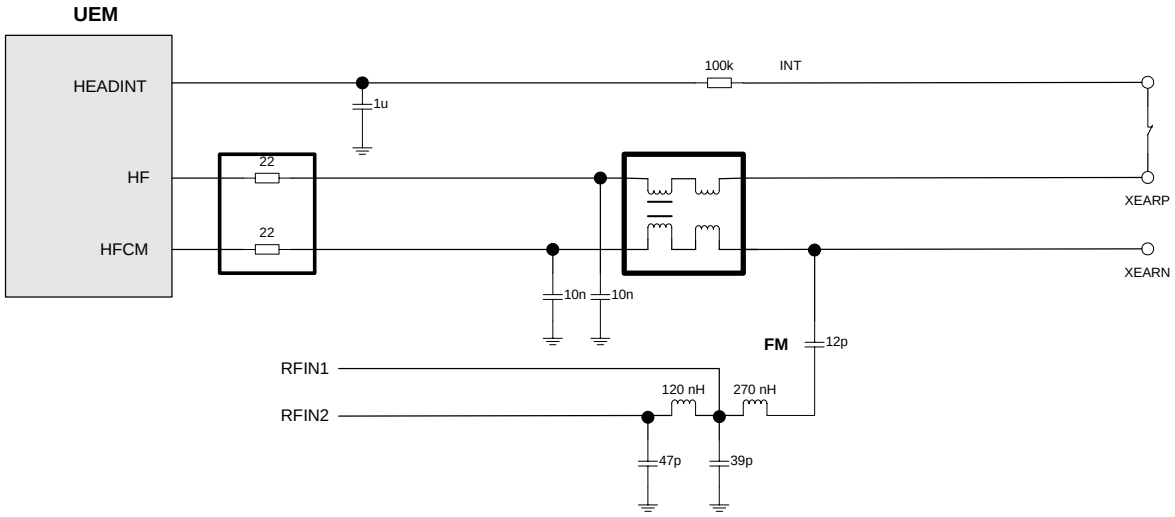
FM radio

Headset is used as antenna.

Figure 9: FM radio antenna interface



As the chipset and the bottom connector used by Nokia 2300 doesn't support true stereo, the stereo functionality from a radio point of view cannot be used efficiently for playing stereo over headset.

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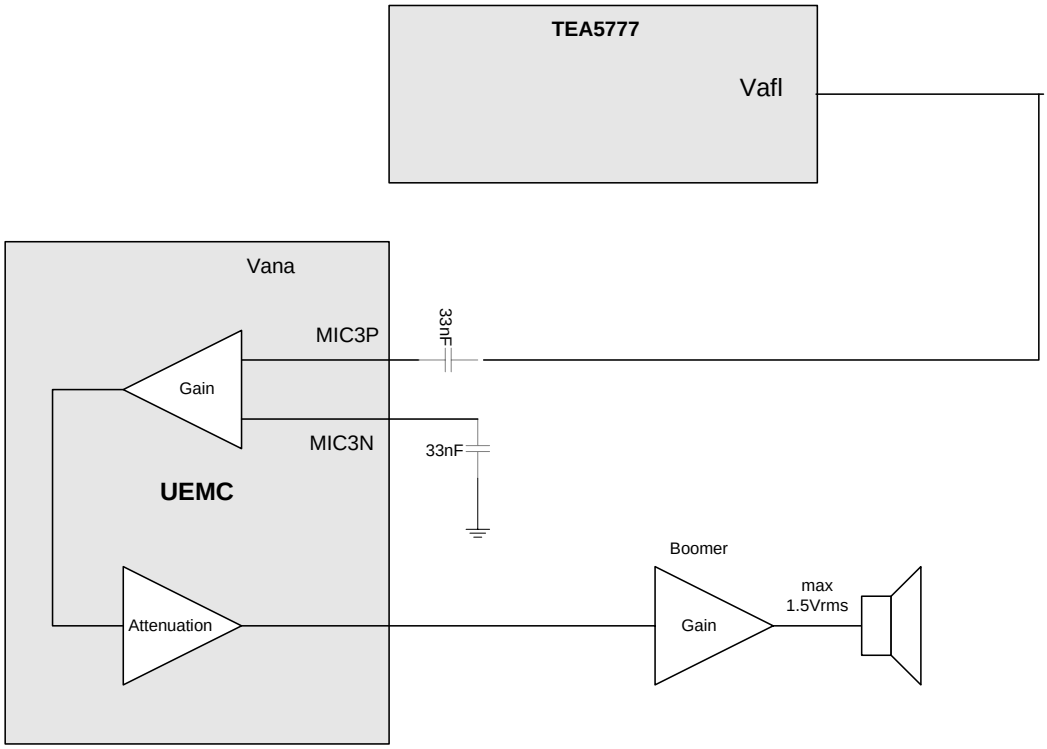
Figure 10: FM radio - BB interface



The nominal output of the radio will be in the order of max. 86mVrms @ 22.5kHz swing, max. 190mVrms @ 50kHz swing, max. 280mVrms @ 75kHz swing. This output is routed as a single ended signal to MIC3P and internally in UEM routed to HF/HFCM (by means of an appropriate routing that either amplifies or provides attenuation). From there, the radio signal is sent to the headset and possibly also the IHF speaker, depending on the user's choice.

The BB interface consist of the following lines:

Data and clock

- Bus_en (GENIO8)

  The data direction is controlled by the edges of the Bus_en signal. Rising edge means reading from the chip, falling edge means writing data into the chip.

- Data (GENIO 12)

- Data clk (GENIO 11)

  Serial clock for data transfer, the rising edge clock the data into the chip

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- Reference clock (GENIO 3)

  The reference clock is 13 MHz.

  The reference clock is only needed when the radio is active. This means that data transfer can be made without having the reference clock active. Using a reference clock of 13 MHz also indicates that the radio will not work if the phone is in sleep modes where the RF reference is turned off.

Audio

- Single ended line signal (Input is MIC3P)

Keyboard

The keyboard PWB layout consists of a grounded outer ring and an inner pad.

The power key is integrated in keypad. The following table shows the principles of the keyboard.

Table 18: Overview of keyboard configuration

UPP Pin	Nokia 2300) Key	In/ Out	Internal Pull Up/down	Interrupt	
GenIO1	0	In	Up	GenIOInt5	Falling edge interrupt
GenIO2/P05	7	In	Up	P0 int	Falling edge interrupt
GenIO20	#	In	Up	GenIOInt2	Falling edge interrupt
GenIO21	*	In	Up	GenIOInt3	Falling edge interrupt
GenIO25	Up	In	Up	GenIOInt4	Falling edge interrupt
GenIO27	1	In	Up	GenIOInt6	Falling edge interrupt
GenIO28	Soft left	In	Up	GenIOInt7	Falling edge interrupt
P00	Menu	In	Up	P0 int	Falling edge interrupt
P01	3	In	Up	P0 int	Falling edge interrupt
P02	9	In	Up	P0 int	Falling edge interrupt
P03	8	In	Up	P0 int	Falling edge interrupt
P04	Down	In	Up	P0 int	Falling edge interrupt
P10	6	In	Up	P1 int	Falling edge interrupt
P11	4	In	Up	P1 int	Falling edge interrupt
P12	Soft Right	In	Up	P1 int	Falling edge interrupt
P13	5	In	Up	P1 int	Falling edge interrupt

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Table 18: Overview of keyboard configuration

P14	C	In	Up	P1 int	Falling edge interrupt
P15	2	In	Up	P1 int	Falling edge interrupt

All lines are configured as input, when there is no key pressed.

When a key is pressed, the specific line where the key is placed is pulled low. This generates an interrupt to the MCU and the MCU now starts its scanning procedure.

When the key has been detected all the keypad-register inside the UPP is reset and it's ready receiving new interrupt.

Display & Keyboard Backlight

LCD Backlight

LCD Backlight consists of 2 sidefirering white LED's which are placed on the display FPC beside the LCD area. They lit into the light guide where the light is distributed to generate sufficient backlight for the LCD & keyboard area.

Keyboard light

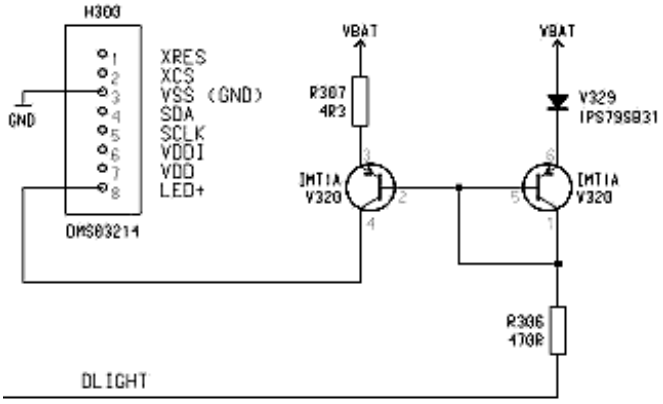
There is no dedicated keyboard light implemented. Keyboard light is provided by the LCD backlight.

LED driver circuit

The LED drivers for the LCD & Keyboard backlight are shown in the following figure.The driver circuit is controlled by the UEM output pin [DLIGHT].

R307 defines the current through the LED’s. Dlight is used for switching on and off the driver. The driver itself controls the current and is temperature compensated.

Figure 11: LED driver circuit for LCD and keyboard backlight



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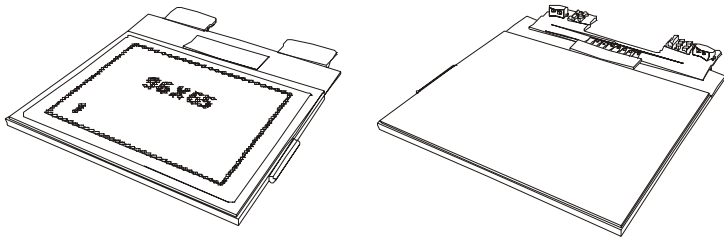
Display

The LCD is a black and white 96x65 full dot matrix display. The LCD cell is part of the complete LCD module, which includes C-cover, gasket, light guide, spring connector, transflector, LEDs and earpiece.

Figure 12: LCD module



The LCD is powered from both V_{FLASH1} and V_{IO}. V_{FLASH1} is used for the boosting circuit and V_{IO} for the driver chip.

Memory Module

The Nokia 2300 baseband memory module consists of external burst flash memory 2Mbyte (16Mbit) (optional: 4Mbyte (32Mbit). The UPP contains internal SRAM with 2 Mbit.

SIM Interface

The whole SIM interface is located in the two ASICs, UPP and UEM.

The SIM interface in the UEM contains power up/down, port gating, card detect, data receiving, ATR-counter, registers and level shifting buffers logic. The SIM interface is the electrical interface between the Subscriber Identity Module Card (SIM Card) and mobile phone (via UEM device).

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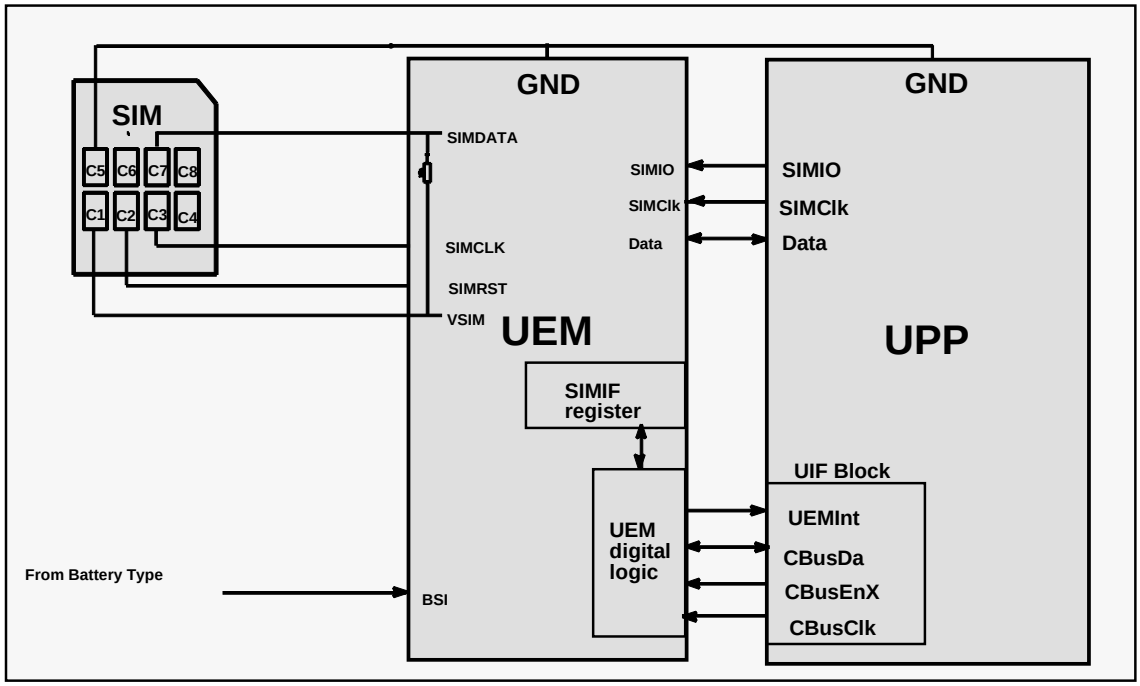
Figure 13: UEM & UPP SIM connections



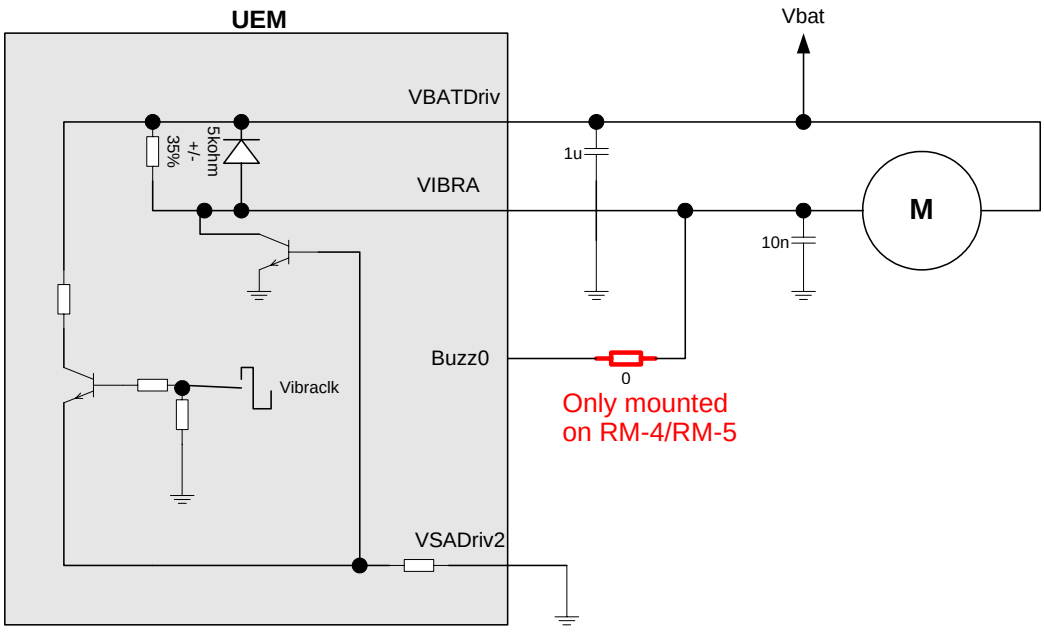
Vibra

The vibra is placed in the bottom of the phone.

The vibra is controlled from the UEM by a PWM (Pulse Wide Modulated) square wave signal.

In Nokia 2300 Duty cycle is 40.5% if the Vbat is less than 4.0 volts otherwise it will be set to 34.3%. PWM is 520 Hz.

Figure 14: Vibra driver circuit



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Test Interfaces

Production test pattern is placed on the engine PWB, for service and production purposes. The same test pattern is used for after sales purposes as well.

Through MBUS or FBUS connections, the phone HW can be tested by PC software (Phoenix) and production equipment (FLALI/FINUI/LABEL).

The testpads are listed in the schematic diagrams.

Connections to Baseband

The flash programming box, FPS8, is connected to the baseband using a galvanic connector or test pads for galvanic connection. The UEM watchdog is disabled during flash programming to prevent a hardware reset of the timer. The flash programming interface connects the flash prommer to the UPP via the UEM and the connections correspond to a logic level of 2.7 V. The flash prommer is connected to the UEM via the MBUS (bi-directional line), FBUS_TX, and FBUS_RX. The programming interface connections between the UEM and the UPP constitute the MBUS, FBUS_TX, and FBUS_RX lines. The interface also uses the BSI (Battery Size Indicator).

FLASH Interface

Flash programming in production is done through the production test pattern (J396) on the PWB.

Table 19: Flash interface signals

Signal	Min	Nom	Max	Note
TX_D		2.7V 0V	3.0V	
RX_D		2.7V 0V	3.0V	
GND		0V		
SCK		2.7V 0V	3.0V	
VPP	0V		12V	Flash programming voltage
BSI	0V		2.7V	Battery size indication. Falling edge required for flash programming.

FBUS Interface

FBUS is an asynchronous data bus having separate TX and RX signals. The default bit rate of the bus is 115.2 kbit/s. FBUS is mainly used for controlling the phone in production. Typical VFLASH1 is 2.78V

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Table 20: FBUS interface signals

Signal		Min	Nom	Max	Note
FBUS_TX	Voh	0.7*VFLASH1		VFLASH1	
	Vol	0		0.3*VFLASH1	
FBUS_RX	Vih	0.7*VFLASH1		VFLASH1	
	Vil	0		0.3*VFLASH1	
Rise time	Tr			12.5 ns	for TX and RX signals
GND			0		

MBUS Interface

The MBUS interface is used for controlling the phone in R&D and CCS. It is a bi-directional serial bus between the phone and PC. In production, the phone initialisation is made using MBUS. The default transmission speed is 9.6 kbit/s.

Table 21: MBUS interface signals

Signal		Min	Nom	Max	Note
GND			0		
MBUS	Vih	1.95V	2.7V	3.0V	bi-directional
	Vil	0V	0.2V	0.83V	
	Voh	1.95V	2.78V	2.83V	
	Vol	0V	0.2V	0.83V	

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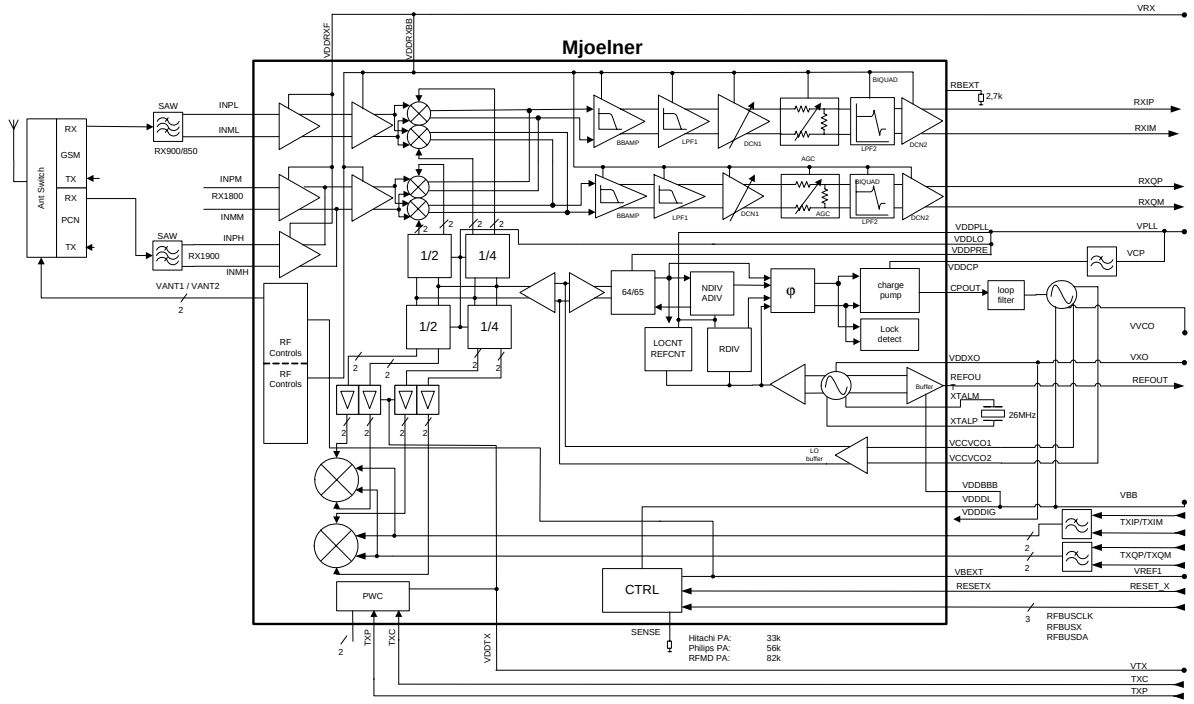
General description of the RF circuits

In the following general description the different parts is described at block level.

Receiver signal path

The signal from the antenna pad is routed to the RX/TX switch (Z700). If no control voltages are present at VANT2 and VANT1, the switch works as a diplexer and the GSM900 signal is passed through the RX/TX switch to the GSM-RX and the GSM1800 signal to PCS-RX.



From the RX/TX switch, the GSM900 signal is routed to the SAW filter (Z602). The purpose of the SAW filter is to provide out-of band blocking immunity and to provide the LNA I Mjoelner (N600) with a balanced signal. The front end of Mjoelner is divided into a LNA and a Pre-Gain amplifier before the mixers.

The output from the mixer is fed to the baseband part of Mjoelner, where the signals are amplified in the BBAMP and lowpass filtered in LPF1 before the DC compensations circuits in DCN1. The DCN1 output is followed by a controlled attenuator and a second lowpass filter LPF2. The output from LPF2 is DC centered in DCN2 before being feed to the BB for demodulation.

The GSM1800 signal chain is similar to GSM900, the SAW filter is numbered Z601.

Transmitter signal path

The I/Q signal from the BB is routed to the modulators for both 900 and 1800 MHz. The output of the modulators is either terminated in a SAW filter (Z603) for GSM900 or a balun for GSM1800.

The signal is then amplified in the PA (N700) where the gain control takes place. The TX signal from the couplers is fed to the RX/TX switch, used to select which signal to route to the antenna.

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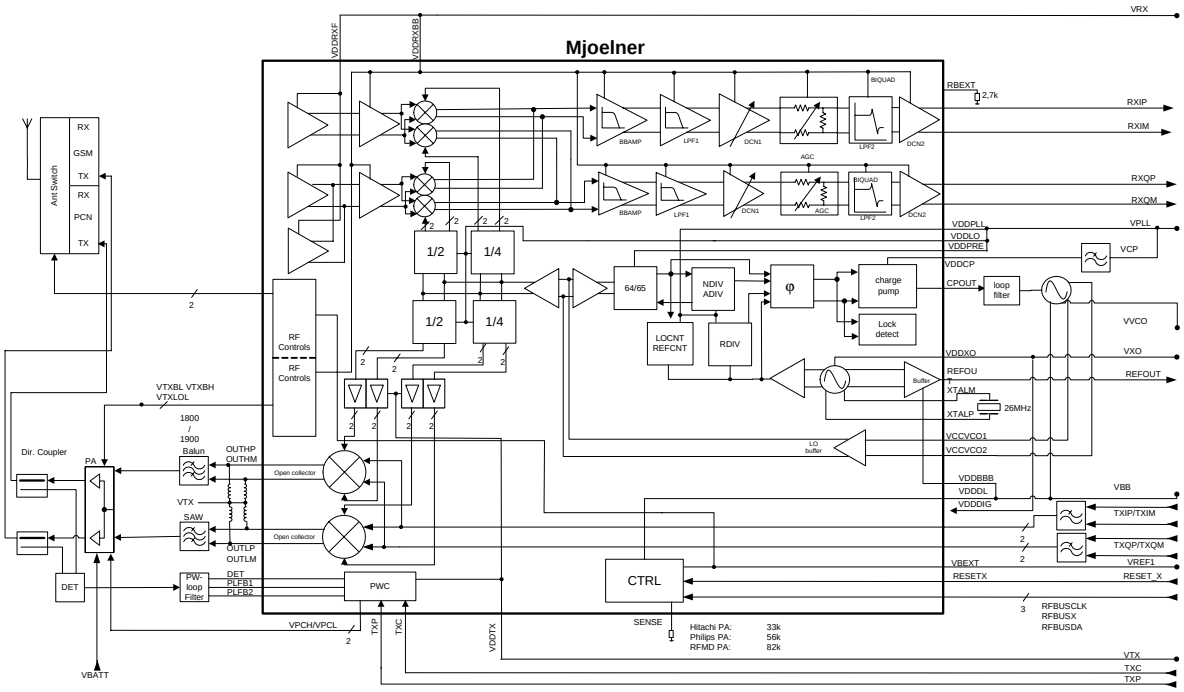

PLL

The PLL supplies Local Oscillator (LO) signals for the RX and TX mixers. In order to be able to generate LO-frequencies for the required EGSM and PCN channels, a regular synthesizer circuit is used. All blocks for the PLL except for the VCO, reference X-tal and lopp filter is located in the Mjoelner IC.

The reference frequency is generated by a 26 MHz Numerically controlled X-tal Oscillator (NCXO), which is located in the Mjoelner IC. Only the X-tal is external. 26 MHz is supplied to BB, where a divide-by-2 (located in the UPP IC) generates the BB-clock at 13 MHz. The reference is supplied to the reference divider (RDIV), where the frequency is divided by 65. The output of RDIV (400kHz) is used as a reference clock for the Phase Detector (φ).

The PLL is a feedback control system controlling the phase and frequency of the LO signal. Building blocks for the PLL include: Phase detector, Charge Pump, Voltage Controlled Oscillator (VCO) and loop filter. As mentioned earlier, only the VCO and loop filter is external to the Mjoelner IC.

The VCO (G600) is the component that actually generates the LO frequency. Based on the control voltage input, the VCO generates a single-enede RF output. The signal is then differentiated through a balun. The signal is fed to the Pre-scaler and N-divider in Mjoelner, these 2 blocks will together divide the frequency by a ratio based on the selected channel.

The divider output is supplied to the phase detector, which compares the frequency and phase of the 400 kHz reference clock. Based on this comparison, the phase detector controls the charge pump to either charge or discharge the capacitors in the loop filter. By charging/discharging the loop filter, the control voltage to the VCO changes and the LO frequency will change. Therefore the PLL keeps the LO frequency locked to the 26 MHz NCXO frequency.

The loop filter consists of the following components: C639-C640-C641 and R618-R619.

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The PLL is operating at twice the channel center frequency when transmitting or receiving in the GSM1800 band. For the GSM900 band the PLL is operating at 4 times the channel frequency. Therefore divide-by-2 and divide-by-4 circuits are inserted between the PLL and output and the LO input for the GSM900 and GSM1800 mixers.

Item	EGSM900	GSM1800
Receive frequency range	925…960 MHz	1805…1880MHz
Transmit frequency range	880…915 MHz	1710…1785MHz
Duplex spacing	45 MHz	95 MHz
Channel spacing	200 kHz	
Number of channels	174	374
Power class	4 (2 W peak)	1 (1 W peak)
Number of power levels	15	16

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